# Designing and Testing an Ultrasonic Sensor

Omar X. Avelar, Omar de la Mora & Diego Romero

## **ANALOG ELECTRONIC SYSTEMS (ECCS 394)**

Instituto Tecnológico y de Estudios Superiores de Occidente (ITESO) Departamento de Electrónica, Sistemas e Informática (DESI)

#### ABSTRACT

A digital ultrasonic sensor will be built and designed by using a piezoelectric transducer, it will be capable of locating nearby objects.

#### **INTRODUCTION & KEY NOTIONS**

Ultrasound is defined as a periodic sound pressure with a frequency greater than the upper boundary of the human hearing, typically greater than 20 kHz.

Various current technologies make use of ultrasonic waves, some examples are material testing or medical use. In this report we will be using it to what is known as ultrasound identification (UID).

UID devices conform a part of real time locating systems (RTLS) where the objects in the neighborhood are used to bounce back the signal and then with some calculations obtain information of their position (Fig. 1).



Fig. 1: UID Principle.

Because ultrasound signals have short wavelengths the sensors are confined for more precise locations.

#### DESIGN

The required stages for our sensor will be summarized by block diagram. (Fig. 2).



Fig. 2: Block diagram.

The emitter and receiver will operate at a frequency of approximately 40 KHz (. The components to be used are labeled as TC-T40-16 and after some measurements we can see they have an impedance of around 1.2  $\Omega.$ 

There are two main analog blocks in this system;

**a)** The filter – which will be a low-pass 50 kHz filter to prevent aliasing in the analog-to-digital conversion.

**b) Amplifier** – that needs to amplify and give enough power to the piezoelectric sender.

ITESO

By: Omar X. Avelar, Diego I. Romero & Omar de la Mora.

Instituto Tecnológico y de Estudios Superiores de Occidente (ITESO), Periférico Sur Manuel Gómez Morín 8585, Tlaquepaque, Jalisco, México, C.P. 45090. Departamento de Electrónica, Sistemas e Informática (DESI).

The low-pass filter will be implemented with a 4<sup>th</sup> Order Sallen-Key topology by cascading two 2<sup>nd</sup> Order stages (Fig. 3).

 $v_{in} \sim C_2$ 

Fig. 3: 2nd Order Sallen-Key.

And finally, the amplifier stage will include a non-inverting amplifier coupled with a Class B stage in crossover-distortion correction feedback configuration (Fig. 5).



Fig. 4: Non-inverting amplifier with power output.

The filter to implement will be Butterworth, so according to the normalized tables:

Stage	ai	bi	Qi
1 <sup>st</sup>	1.8478	1.0000	0.54
2 <sup>nd</sup>	0.7654	1.0000	1.3100

Where in relationship to the previous table, the transfer function is shown in equation (1).

$$H(s) = \frac{1}{b_1 s^2 + a_1 s + 1} \tag{1}$$

where for a Sallen-Key configuration with unity gain;

$$b_{i} = C_{1}C_{2}R_{2}R_{3} \quad , \quad \omega_{o} = \frac{1}{\sqrt{b_{i}}} = \frac{1}{\sqrt{C_{1}C_{2}R_{2}R_{3}}} \quad \text{or}$$

$$f_{o} = \frac{1}{2\pi\sqrt{R_{1}R_{2}C_{1}C_{2}}} \quad \text{and} \quad Q = \frac{\sqrt{R_{1}R_{2}C_{1}C_{2}}}{(R_{1}+R_{2})C_{2}}$$

We start by calculating the values or the **first** stage:

$$C_1 = 1$$
 ,  $C_2 = n$  ,  $R_1 = R$  ,  $R_2 = mR$ 

then  $\omega_o = 1$  and  $m = \frac{1}{2\pi \omega_o QR} - 1$  .

If we define R = 0.1 then m = 1.947 and  $n = \frac{1}{m} \left(\frac{1}{2 \pi R \omega_o}\right)^2 = 1.30$ .

And finally for the **second** and final stage:

$$C_1 = 1$$
 ,  $C_2 = n$  ,  $R_1 = R$  ,  $R_2 = mR$  .

then  $\omega_o = 1$  and  $m = \frac{1}{2\pi \omega_o QR} - 1$ .

If we define R = 0.01 then m = 11.149 and  $n = \frac{1}{m} \left(\frac{1}{2 \pi R \omega_o}\right)^2 = 22.72$ .



Instituto Tecnológico y de Estudios Superiores de Occidente (ITESO), Periférico Sur Manuel Gómez Morín 8585, Tlaquepaque, Jalisco, México, C.P. 45090. Departamento de Electrónica, Sistemas e Informática (DESI). Ultrasonic Sensor

By: Omar X. Avelar, Diego I. Romero & Omar de la Mora.

And zooming in (Fig. 7) we can see a correct functionality in the desired frequency range.

## The normalized values to 1 Hz then can be summarized in the following tables.

1st Stage					
$R_1$	0.1 Ω	$R_2$	0.1947 Ω		
$C_1$	1 F	$C_2$	1.3 F		

2nd Stage					
$R_1$	0.01 Ω	$R_2$	0.01 Ω		
$C_1$	1 F	$C_2$	22.72 F		

Normalizing to commercial values (Fig. 5) with software we obtain:



Fig. 5: 4th Order Butterworth low-pass filter @ 50 kHz.

#### With a frequency response in the next figures (Fig. 6 & Fig. 7).





Since the system will be fed a square signal of 3.3 Volts in amplitude with the first fundamental frequency of  $40\,kHz$ , then the amplifying stage will have an approximate gain of  $3\,V/V$ , therefore the following circuit will be implemented (Fig. 7).



Fig. 8: Amplifier and power stage.

With the amplified pulse on our emitter we are able to increase the range of the sensor.

#### Subject: Analog Electronic Systems - Page 3 of 4 Guadalajara, Mexico // Thu, May 21, 2009.



Instituto Tecnológico y de Estudios Superiores de Occidente (ITESO), Periférico Sur Manuel Gómez Morín 8585, Tlaquepaque, Jalisco, México, C.P. 45090. Departamento de Electrónica, Sistemas e Informática (DESI).

### **Ultrasonic Sensor**

By: Omar X. Avelar, Diego I. Romero & Omar de la Mora.

#### CONCLUSIONS

Analog systems and implementations are greatly required on every-day devices. The mixing of analog and digital systems offer a great combination in the field of applied electronics. One thing to take note is that moderately cheap and really innovative appliances can be built with well thought and designed systems.

Ultrasound detection can be greatly improved with well thought processing algorithms that make up for defects in the simplest method, while analog maintain special properties such as continuous-time speed (in a sense) and some implementations may be cheaper which helps reduce the overall system cost.

#### REFERENCES

[1] R.C. Jager, Microelectronic Circuit Design, New York, NY: Mc-Graw Hill, 1997.

[2] Ron Mancini, Op Amps For Everyone, Texas Instruments, August 2002.

[3] A. S. Sedra and K. C Smith, Microelectronic Circuits. New York, NY: Oxford University Press, 2003.

[4] R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, New York, Wiley Interscience, 1997.