Designing a Pipelined Architecture 4 Bit ADC

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ANALOG ELECTRONIC SYSTEMS (ECCS 394)

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DESCRIPTION

The design consists of a 4 Bit analog to digital converter (ADC). We will be implementing a pipeline architecture. Currently in contrast with other ADC types, this segment is widely used in high speed applications (Fig. 1).

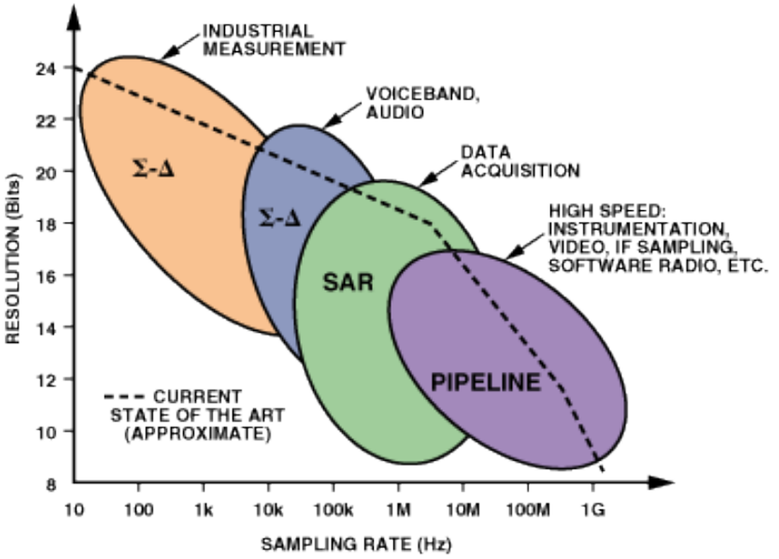

Fig. 1: ADC architectures comparative,
Image courtesy from National Semiconductors.

The pipeline architecture offers great balance between silicon size, speed, resolution and analog design effort in contrast to other data-acquisition systems.

As you can see from Fig. 1 the resolution achieved with it can be enough for most applications while reducing costs and keeping a high-speed operation available.

Now, lets take a closer look at the pipeline architecture, basically it has multiple sequential stages that make the conversion more precise by chaining the voltage comparisons, then taking off the residue of the signal and comparing it again, this process is better visualized in the next figure (Fig. 2).

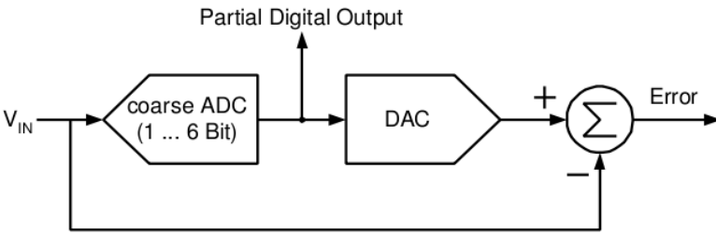

Fig. 2: Single stage of a pipelined ADC.

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DESIGN

The design consists of three main blocks:

(1) - **Sample and hold** circuit (Fig. 3).

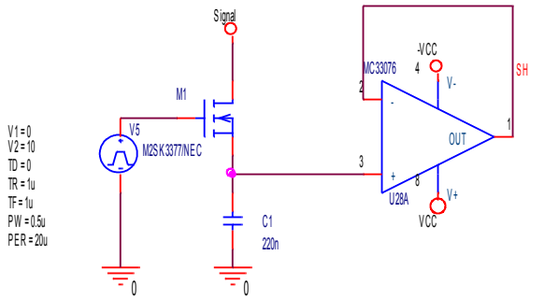

Fig. 3: Sample & Hold @ 50 KHz.

(2) - **1 Bit coarse ADC** (Comparator – Fig. 4).

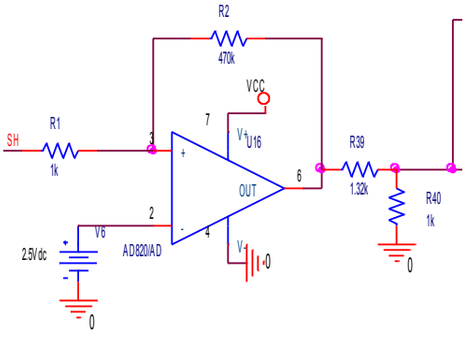

Fig. 4: Comparator.

(3) - **Adder and Amplifier** (Fig. 5).

The description of each stage is as follows.

According to our block diagram from Fig. 2, we first need to pass the signal by a comparator, to do so the original analog signal must be *sampled and held* **(1)** so the *comparator* **(2)** is fed a stable signal. After the first bit is obtained, it needs to be subtracted **(3)** from the original signal to obtain the residue that will be entering the next conversion stage. The residue will also be amplified **(3)** to remain in the full-scale range of the comparator to reduce loss of resolution.

Each portion of the comparator outputs a Bit of the data converter and every single output will contain a latch (Fig. 6).

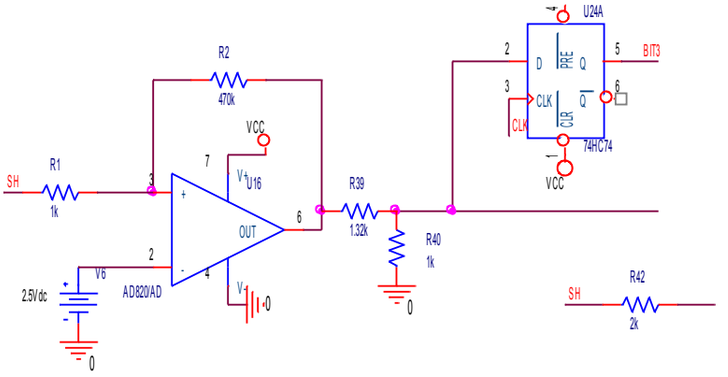

Fig. 6: Latch shown on the top right.

The required pipelined data converter has a resolution of 4 Bits, each stage with an ADC of 1 Bit - therefore the design it will contain:

- 1 Sample & Hold.
- 4 Latches.
- 4 comparators.
- 3 Adders and amplifiers.

The full organized stages for the design are shown in the next page (Pag. 3).

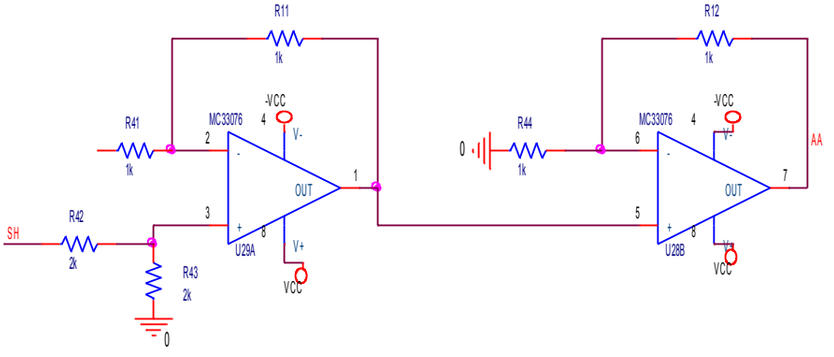

Fig. 5: Adder and Amplifier.

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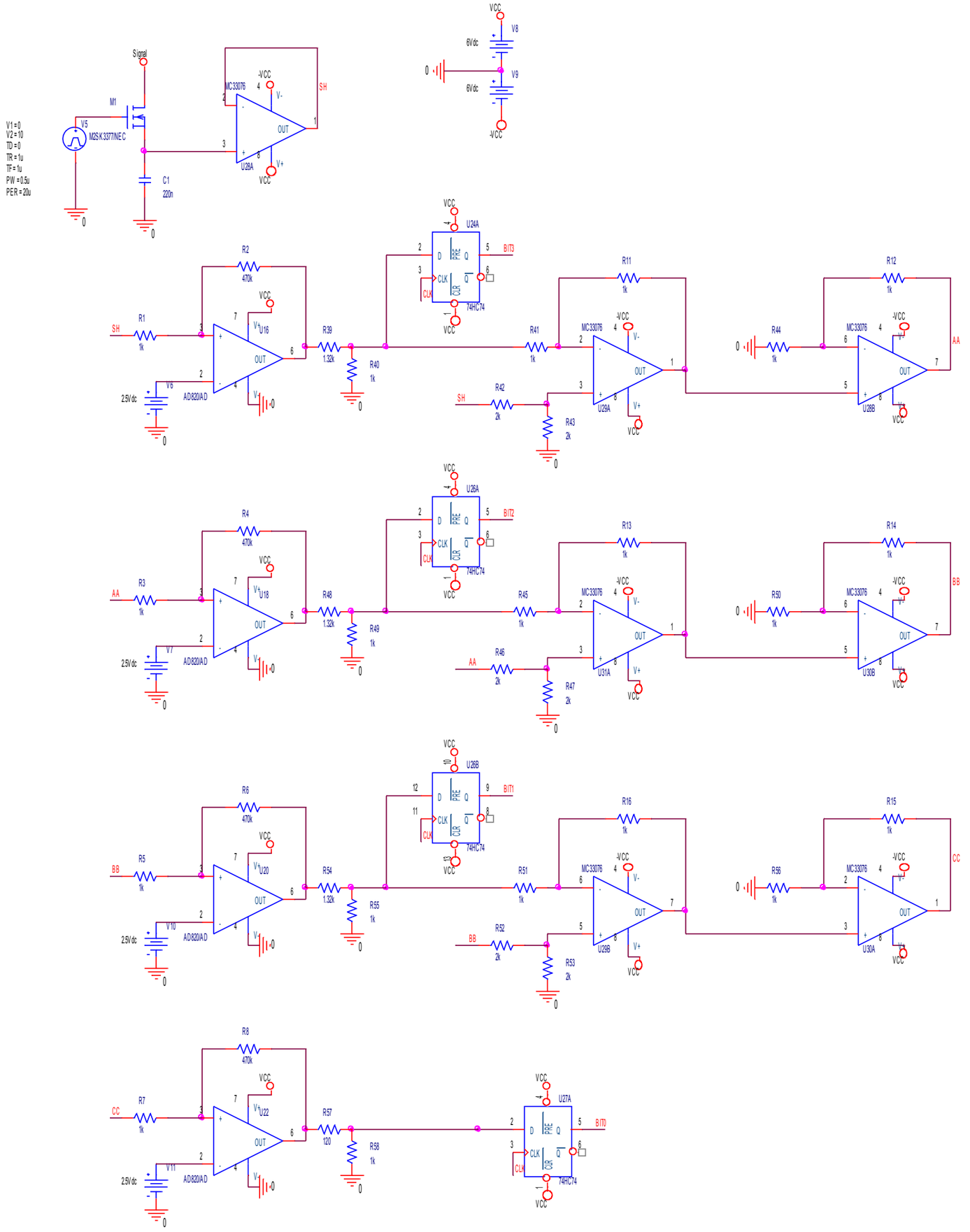

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SIMULATION & TESTING

We will be using SPICE to test our previous design. We start by putting a sine-wave of 1 Khz at the input (Fig. 8).

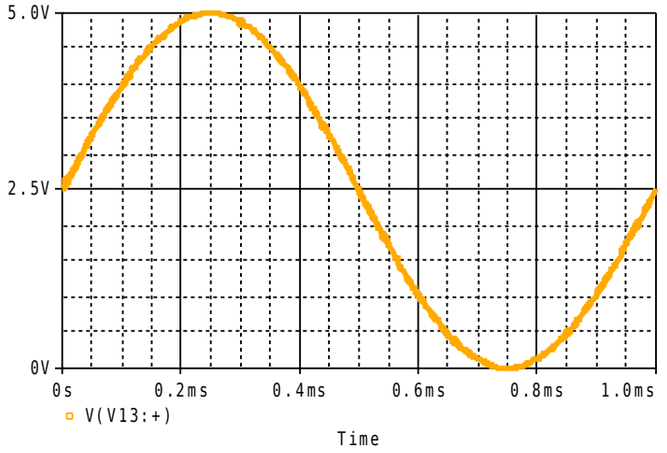

Fig. 7: Sine-wave at input.

Then, we check the sample and hold stage,

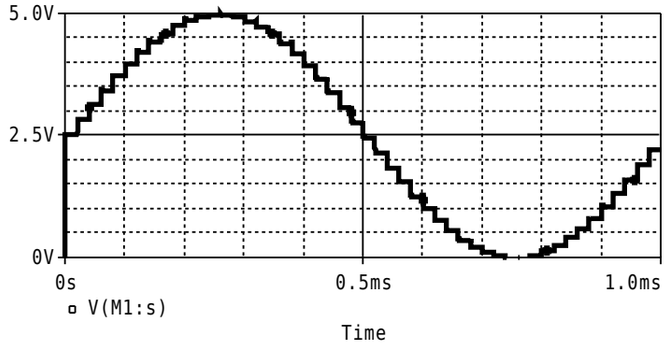

Fig. 8: After the sample and hold circuit.

So far everything is working as expected, the next portion of the simulation will display the amplified residue of the first stage as the input is the same sine-wave (Fig. 9).

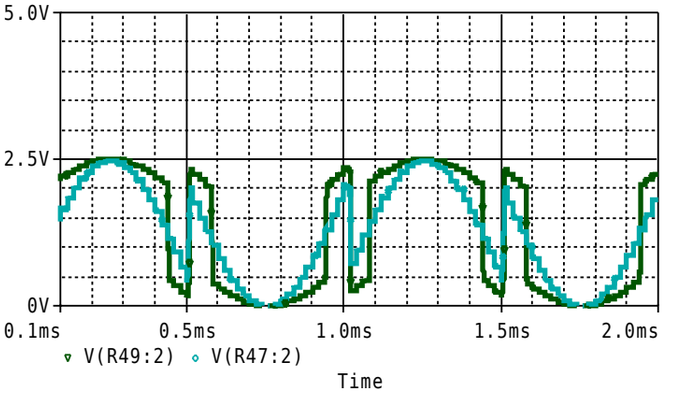

Fig. 9: Signals to subtract from each-other.

Fig. 9 – Reduced in amplitude to achieve a suitable result in the residue.

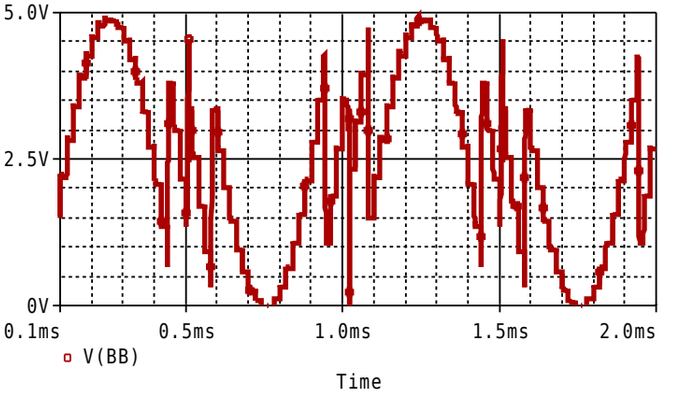

Fig. 10: Amplified residue of first stage.

We can clearly see how the residue was amplified (twice in this case) to make use of the full-scale voltage.

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Now, to analyze each latched bit-stream as input signal is the same sine-wave (Fig. 11).

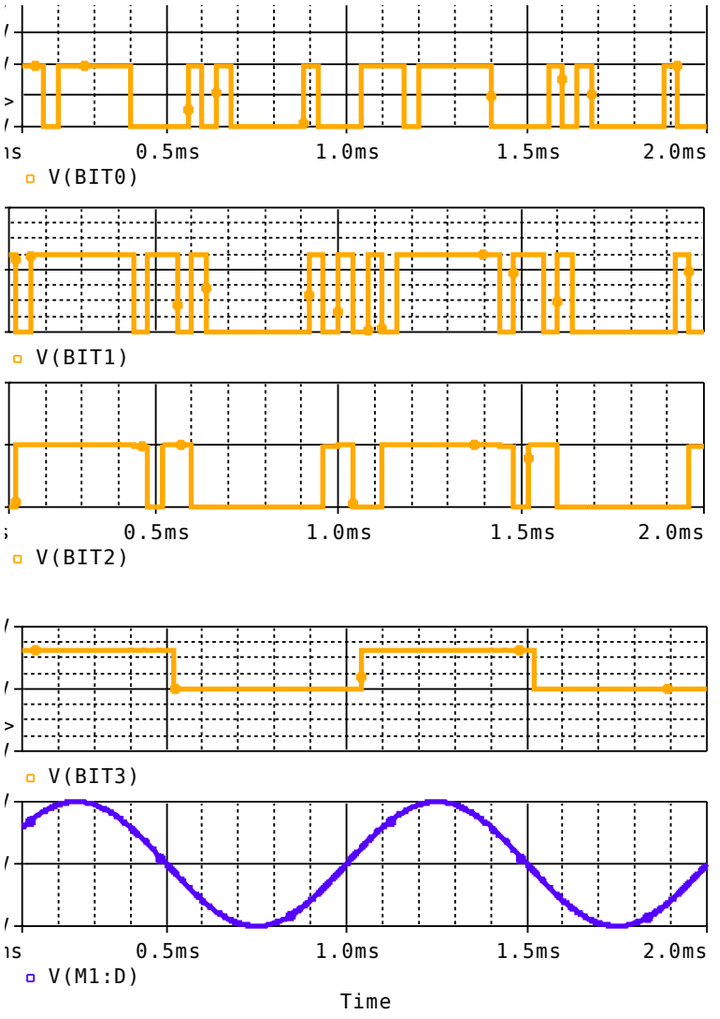

Fig. 11: Digital outputs vs. Sine-wave input.

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Now to look at the digital reconstruction from the digital signal, we feed the word onto a R2R DAC (Fig. 12).

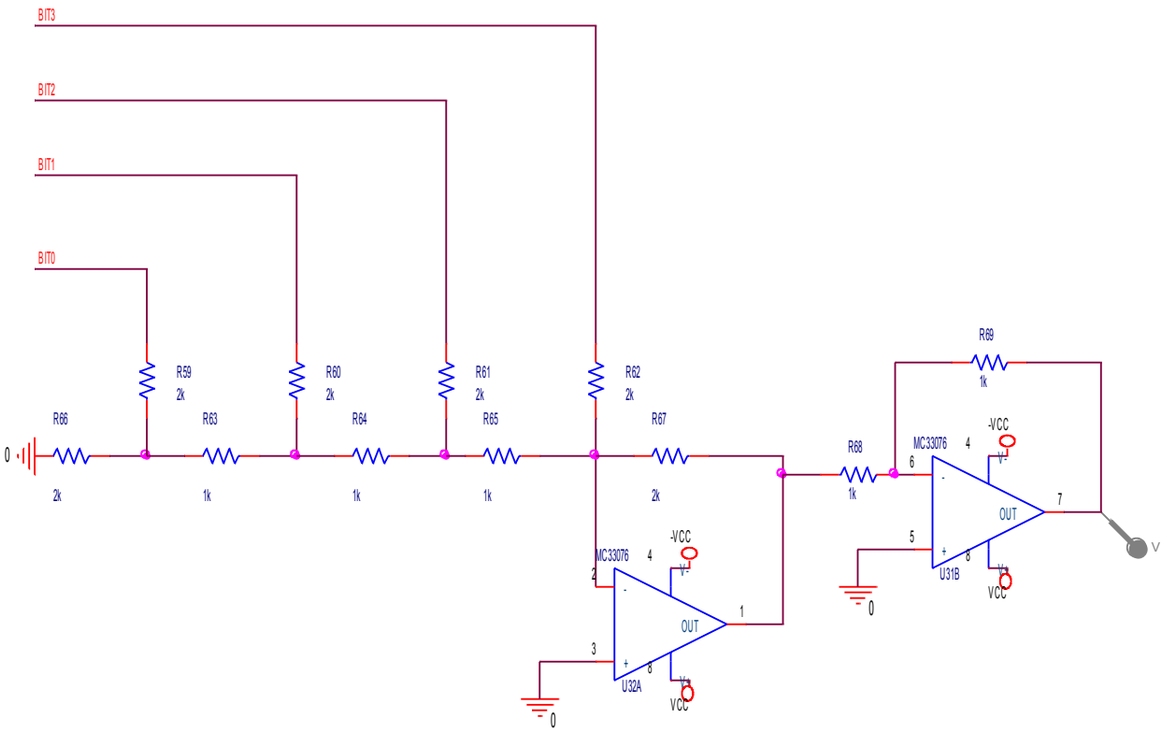

Fig. 12: R2R DAC.

We can observe the 16 Bit represented signal according to their respective signals (Fig. 13 & Fig. 14).

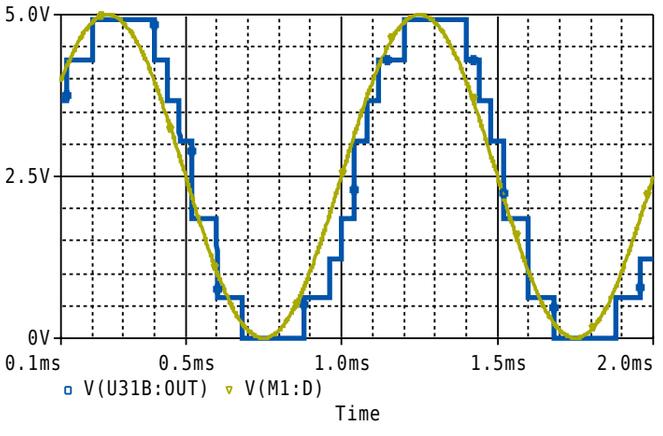

Fig. 13: Original vs Digital (Sine-wave).

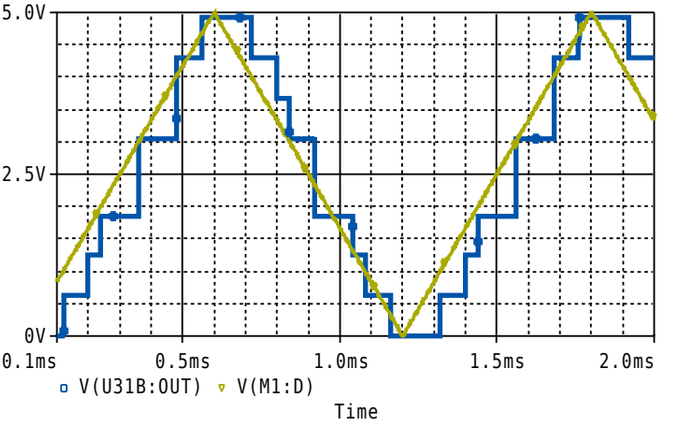

Fig. 14: Original vs Digital (Triangular wave).

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After noticing we are only getting 7 plus zero effective steps (Fig. 13 and 14), we decided to quadruple the sampling frequency (200 KHz) and the latch clock to 41.66 KHz, we get the following results (Fig. 15 & Fig. 16).

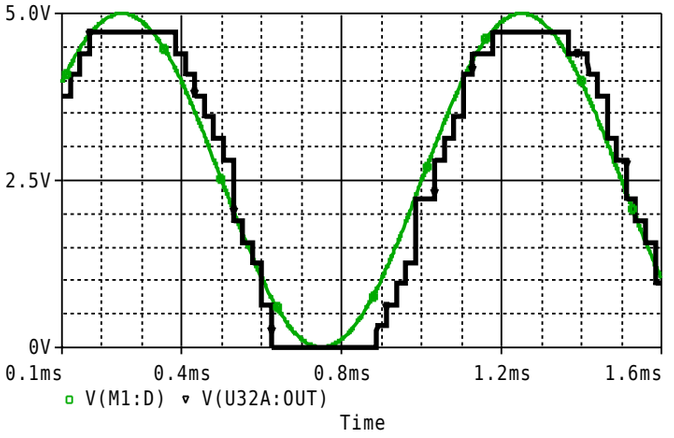

Fig. 15: Sine-wave reconstruction.

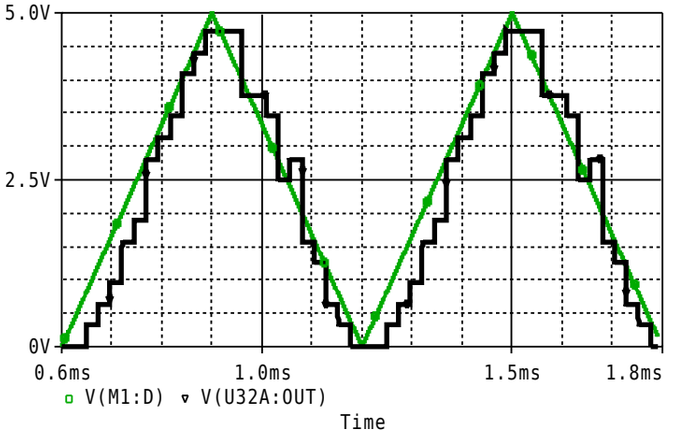

Fig. 16: Triangular wave reconstruction.

As we can see, in both cases (Fig. 15 & Fig. 16), the number of steps jumped to 11 plus zero, hence the data converter has an approximate full resolution of: **3.58 Bits** which is still relatively less than the expected 4 Bit resolution, but it does not account for a full Bit lost like the first experiment**.**

CONCLUSIONS

We experimented with various designs and practiced our block-by-block design process. It was interesting to look for optimal ways of doing certain things such as picking a low internal capacitance transistor for the sample and hold circuit to picking fast and rail to rail operational amplifiers, it was a nice experience overall to use our acquired knowledge over the courses.

We also experienced some problems with the simulation software such as LTSpice or Cadence's Allegro // OrCAD as it had problems simulating certain behavior on certain components, so we either had to replace and look for a similar component or find why the error was being caused.

Something that needs to be taken not for granted is the latches at the digital outputs as it makes our system more digitally stable and less prone to oscillations.

REFERENCES

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